

In Claims:

Cancel claims 23, 25, 31 and 32 without prejudice.

Rewrite the pending claims and add new claims to read as follows:

1. (Currently Amended) A semiconductor package, comprising:
a chip carrier to receive a semiconductor with a dimension greater than 26 mm, said chip carrier having a first coefficient of thermal expansion different than the coefficient of thermal expansion of said semiconductor; and
a stress inhibiting intermediate mounting substrate connected to said chip carrier through a first array of solder connections, said stress inhibiting intermediate mounting substrate being adapted for connection to ~~an interposer~~ a printed circuit board through a second array of solder connections, said stress inhibiting intermediate mounting substrate having a second coefficient of thermal expansion different than the coefficient of thermal expansion of said chip carrier and smaller than the coefficient of thermal expansion of said ~~interposer printed circuit board~~, and said stress inhibiting intermediate mounting substrate being adapted for allowing access through the substrate to one or more solder connections in the first array.
2. (Currently Amended) The semiconductor package of claim 1 wherein said ~~interposer stress inhibiting intermediate mounting substrate~~ is a printed circuit board.
3. (Original) The semiconductor package of claim 1 wherein said chip carrier is formed of a ceramic material.
4. (Original) The semiconductor package of claim 3 wherein said chip carrier has a CTE between 3 and 7 PPM.
5. (Original) The semiconductor package of claim 1 wherein the first coefficient of thermal expansion is larger than the coefficient of thermal expansion of said semiconductor.
6. (Original) The semiconductor package of claim 1 wherein the second coefficient of thermal expansion is larger than the coefficient of thermal expansion of said chip carrier.
7. (Original) The semiconductor package of claim 5 wherein the second coefficient of thermal expansion is larger than the coefficient of thermal expansion of said chip carrier.

8. (Original) The semiconductor package of claim 6 wherein the second coefficient of thermal expansion is smaller than the coefficient of thermal expansion of said printed circuit board.
9. (Original) The semiconductor package of claim 1 wherein the second coefficient of thermal expansion is between 14 and 18 PPM.
10. (Original) The semiconductor package of claim 1 further comprising solder bumps positioned on said chip carrier to facilitate connection with said semiconductor.
11. (Original) The semiconductor package of claim 10 wherein the solder bumps are lead-free.
12. (Original) The semiconductor package of claim 1 wherein at least one solder connection is lead-free.
13. (Original) The semiconductor package of claim 1 further comprising a semiconductor having a dimension greater than 26 mm mounted to the chip carrier.
14. (Currently Amended) The semiconductor package of claim 1 further comprising under-fill resin positioned between said ~~solder bumps~~ first array of solder connections.
15. (Original) The semiconductor package of claim 1 further comprising a lid positioned over said chip carrier.
16. (Original) The semiconductor package of claim 1 wherein said stress inhibiting mounting substrate includes signal paths between a top surface of said stress inhibiting mounting substrate and a bottom surface of said stress inhibiting mounting substrate.
17. (Currently Amended) A semiconductor package comprising:
 - a chip carrier to receive a semiconductor said semiconductor having a dimension greater than 26 mm and said chip carrier having a first coefficient of thermal expansion between 3 and 7 PPM; and
 - a stress inhibiting mounting substrate connected to said chip carrier through a first array of solder connections, said stress inhibiting intermediate mounting substrate being adapted for allowing access through the substrate to one or more solder connections in the first array.

18. (Original) The semiconductor package of claim 17 wherein said stress inhibiting mounting substrate has a coefficient of thermal expansion between 14 and 18 PPM.
19. (Original) The semiconductor package of claim 17 further comprising a printed circuit board mounting substrate connected to said stress inhibiting mounting substrate through a second array of solder connections, said printed circuit board mounting substrate having a coefficient of thermal expansion between 14 and 17 PPM.
20. (Original) The semiconductor package of claim 18 further comprising a printed circuit board mounting substrate connected to said chip carrier through a second array of solder connections, said printed circuit board mounting substrate having a coefficient of thermal expansion between 14 and 17 PPM.
21. (Currently Amended) The semiconductor package of claim 17 further comprising ~~further comprising~~ a semiconductor having a dimension greater than 26 mm mounted to the chip carrier.
22. (Currently Amended) A semiconductor package, comprising:
a chip carrier to receive which a semiconductor is connected by an array of solder bumps;
a stress inhibiting intermediate mounting substrate connected to said chip carrier through a first array of solder connections, said substrate being adapted for allowing access through the substrate to one or more solder connections.
23. (Canceled) The semiconductor package of claim 22 further comprising further comprising a semiconductor mounted to the chip carrier.
24. (Currently Amended) The semiconductor package of claim 22 further ~~comprises~~ comprising an interposer a printed circuit board connected to said substrate through a second array of solder connections, said ~~interposer~~ printed circuit board being adapted for allowing access through the substrate to one or more solder connections of the first array of solder connections.
25. (Canceled) The semiconductor package of claim 24 wherein said interposer is a printed circuit board.

26. (Original) The semiconductor package of claim 22 wherein said access permits the removal of flux.
27. (Original) The semiconductor package of claim 22 wherein said access permits the cleaning of flux.
28. (Currently Amended) The semiconductor package of claim 22 wherein said access permits the insertion of ~~under-fill~~ underfill material.
29. (Currently Amended) The semiconductor package of claim 22 wherein the substrate further includes ~~at least one additional row~~ a plurality of rows of solder connections ~~adjacent to a row of solder connections of the array of solder connections~~ wherein the number of solder connections in the at least one ~~additional~~ row is less than the number of solder connections in each row of solder connections of a subset of the array plurality of solder connections because of the absence of solder connections at or near one or more corners of the substrate
30. (Currently Amended) A substrate having a through-hole channel located at or near a center of the substrate and a first row plurality of rows of solder connections ~~adjacent to a row of solder connections of an array of solder connections~~ wherein the number of solder connections in a first row is less than the number of solder connections in each row of solder connections of a subset of the array plurality of solder connections because of the absence of solder connections at or near one or more corners of the substrate.
31. (Canceled) A method of underfilling a gap between a multi-sided semiconductor device and a substrate to encapsulate a plurality of electrical connections formed therebetween, comprising:
- forming a channel between said device and said substrate;
 - leaving said channel open to at least one side of said device to permit access to said device; and
 - dispensing an under-fill material adjacent said at least one side of said device through said channel.
32. (Canceled) The method of claim 31 wherein said channel permits the removal of residual flux.

33. (New) The semiconductor package of claim 22 wherein the chip carrier includes a passage allowing access through the chip carrier to one or more solder connections.